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THE FABRICATION OF RIDGE WAVEGUIDED PHOTONIC CIRCUITS WITH CHEMICALLY ASSISTED ION BEAM ETCHED MIRRORS

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The fabrication of etched ridge waveguide based monolithically integrated photonic circuits is described. Etched mirrors are created at the same time as the etched ridge waveguides by means of a one-step two-level etch technique.

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I. Introduction

Discreet GaAs-AlGaAs laser diodes have already proven to be highly useful and commercially viable photonic devices. The next logical step in the evolution of this family of devices is the monolithic integration of photonic devices based on a laser diode heterostructure. The standard optical waveguide structure used to confine and amplify light within a diode laser can also be used as a saturable absorber[1], electro-optic modulator[2], detector[3], and passive waveguide[4]. Applications range from Q-switched and bistable lasers to optical switching and optical logic. This paper reviews the processing techniques used to fabricate laser based logic devices comprised of chemically assisted ion beam etched (CAIBE) waveguides and mirrors.[5,6,7] A brief discussion of principles of guiding within an etched ridge waveguide will precede a chronology of the processing steps.

II. Etched Ridge Waveguides

In order for monolithically integrated optical devices to function, light must be routed to, and confined in each device in accordance with the over all "photonic circuit". The photonic circuits whose fabrication is described in this paper use etched ridge waveguides for both of these requirements. Etched ridge waveguides use index guiding to confine light in the vertical direction and "strip loading" to confine light in the lateral direction. In both cases light is confined by having, at some

distance from the center of the waveguide, a purely imaginary phase constant in the direction normal to the direction of propagation. By definition, this creates an exponential decay of intensity with distance from the center of the guide. This exponential decay is the result of light traveling in phase, along the boundary between a region experiencing a high index of refraction (the core) and a region with a lower index of refraction (the cladding). Since the wave equation for light dictates that the square of the magnitude of the phase constant vector for light traveling in a given material equals the square of the product of the index of refraction and the free space propagation constant,

$$B_x^2 + B_y^2 + B_z^2 = (nk_o)^2 \ , \qquad (1)$$

it follows that, in order for light traveling in both the core and cladding to be constantly in phase ($B_z$core = $B_z$cladding), the phase constants in the directions normal to propagation must be real in the higher index core and imaginary in the lower index cladding. A standard laser heterostructure confines light in the vertical direction in this manner by using planar epitaxially grown layers of varying index of refraction. The strip loading in an etched ridge laser is formed by etching down to just above the planar core on either side of the waveguide. This produces

the equivalent of a slight lateral index drop in the side regions by lowering the phase constant in the direction of propagation of their possible vertical modes.[8] This is more desirable than etching all the way through the core because the smaller index drop allows for wider, and therefore easier to fabricate, single mode lasers.

III. Processing

The laser logic device being fabricated requires etched regions of two different depths: a deep etch that extends well into the lower cladding region for the laser mirrors, and a shallow etch to delineate the waveguides. In order to create an effective lateral index difference, the shallow etch should be within 100 nm of the top of the planar waveguide's core.[9] Both etch depths can be achieved with a single etch by depositing a material which etches slowly in the CAIBE over the shallow etch regions.[6] When this material is totally etched away, the previously uncovered deep etch regions will have already etched down to the difference between the two etch depths. A single layer of SiO_2 can be used as both the etch retarding layer and insulation between the contact pads and the semiconductor. Chromium, whose etch rate in the CAIBE is almost negligible, is used to mask regions which require no etching. These regions correspond to the regions to be metallized, namely the ohmic

contacts on top of the waveguides and the electrical contact pads. For this reason the chromium etch mask is delineated at the same time as the p-type ohmic contact metallization. The entire process requires only two photo-lithographic mask steps. A chronology of the design and processing steps developed at Cornell University utilizing the National Nanofabrication Facility are as follows:[6]

1. The masks used to delineate the SiO_2 and the metallization are laid out on a CAD system.

2. The photolithographic masks are generated using a Mann 360F Pattern Generator.

3. The wafers to be processed are cleaned and dried. These include the laser heterostructure wafers (see Figure 1), along with blank GaAs substrates used for etch depth calibration. SiO_2 is grown on the wafers. The desired thickness of the SiO_2 is determined by the etch rate of both SiO_2 and GaAs/AlGaAs in the CAIBE by the following equation:

$$T_{SiO2} = R_{SiO2} (D / R_{GaAs}) , \qquad (2)$$

where R_{SiO2} is the SiO_2 etch rate, R_{GaAs} is the average heterostructure etch rate, and D is the difference in etch depths.

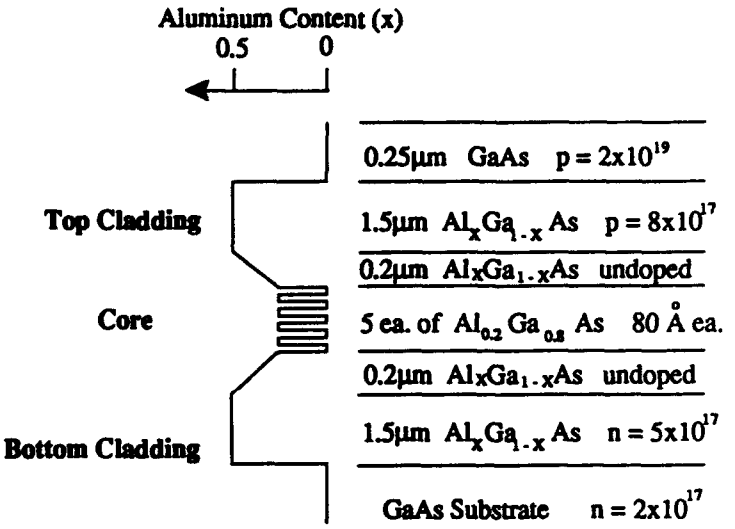

Figure 1. A standard epitaxially grown laser heterostructure, utilizing multiple quantum wells in its active region.

4. Photo-resist is spun on and the first mask pattern is transferred onto the wafers, leaving exposed the areas which are to be deep etched or ohmicly contacted.

5. The wafers are placed in a reactive ion etcher and the SiO_2 in the exposed areas is etched away, using a CHF_3 plasma. While still in the reactive ion etcher, the photo resist is removed with an oxygen plasma. (See Figure 2a.)

6. In order to improve the ohmic contact, a shallow Zn diffusion is used to dope the contact regions p+. $ZnAs_3$ is used to form a Zn vapor source during an open ampule diffusion, lasting 9 minutes at 650 degrees centigrade. The patterned SiO_2 on the wafers insure that only the areas to be p-contacted are doped p+. Since the diffusion is shallow, (~300 nm) the Zn diffusion in the regions to be deep etched is without consequence to the final device.

7. After the diffusion, a new layer of 5214 photo resist is spun on the wafers and the metallization pattern is transferred to the photo resist. Using the negative reversal process for 5214, the areas to be metallized are left uncovered.

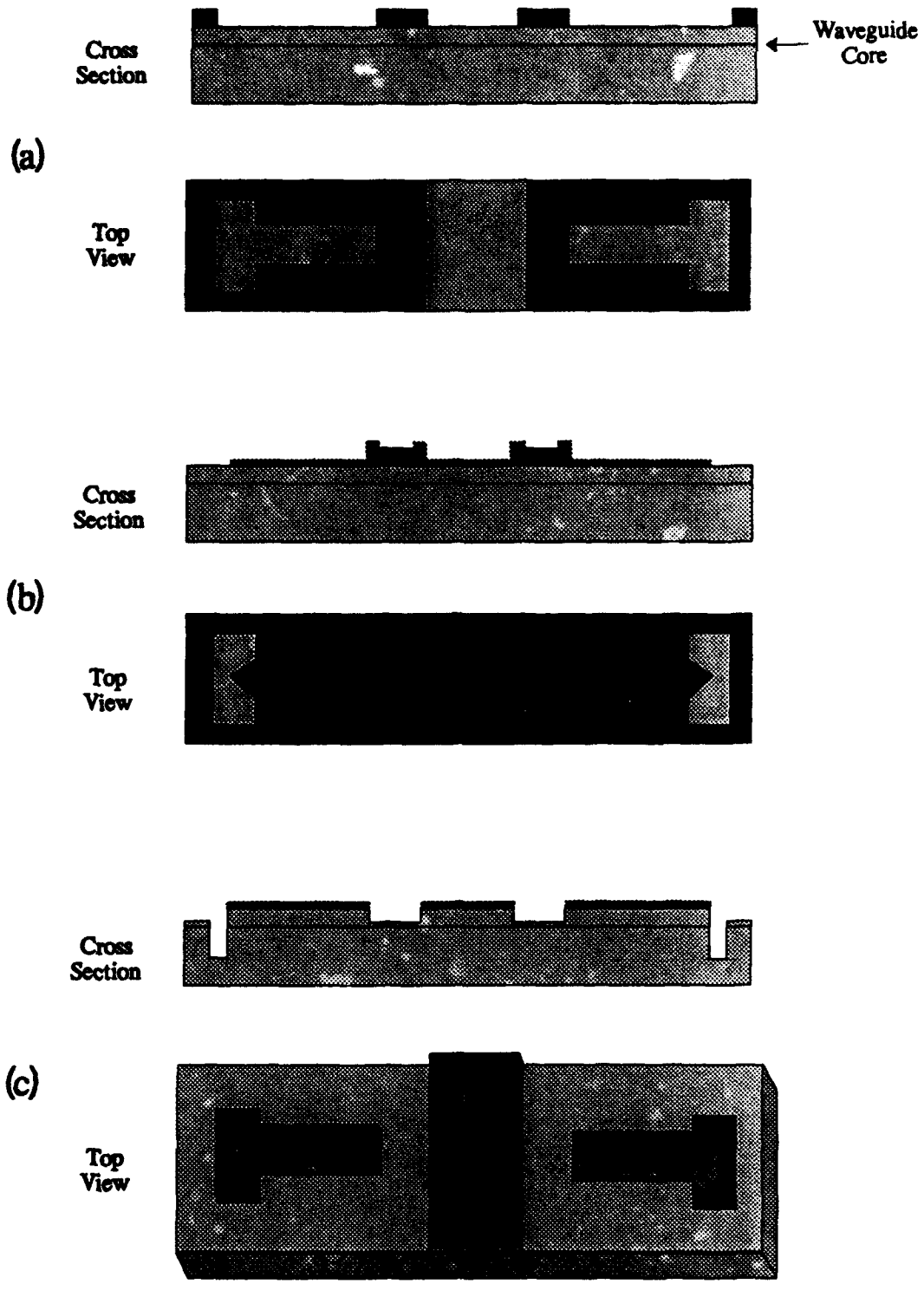

Figure 2. Cross sections and top views of two intersecting laser cavities during progressive stages in fabrication: (a) After the patterning of the SiO_2 etch retarding mask, (b) After the patterning of the ohmic contact metallization / chrome etch mask, and (c) After etching in the CAIBE.

8. A standard GaAs p-type ohmic contact metallization, followed by a 100 nm of chromium, is evaporated onto the sample. The pre-alloyed ohmic contact metallization consists of 20 nm of titanium, 20 nm of platinum, and 200 nm of gold.

9. Soaking in acetone lifts off the metallization in the regions to be etched. (See Figure 2b.)

10. The wafers are dry etched in the CAIBE, starting with the blank GaAs substrates in order to calibrate the etch rates. (See Figure 2c.) The deep and shallow etches, as seen by a scanning electron microscope, is shown in Figure 3.

11. Using 3 micron AlO_3 grit, the backs of the wafers are then lapped down such that the final wafer thickness is approximately 150 microns.

12. The samples are cleaned and dried. A standard n-type ohmic contact metallization is evaporated on the backs of the wafers (10 nm of nickel, 40 nm of germanium, 80 nm of gold, 50 nm of silver, and 80 nm of gold).

13. The wafers are then placed in an alloying oven at 360 degrees centigrade for 60 seconds in order to alloy the ohmic contacts.

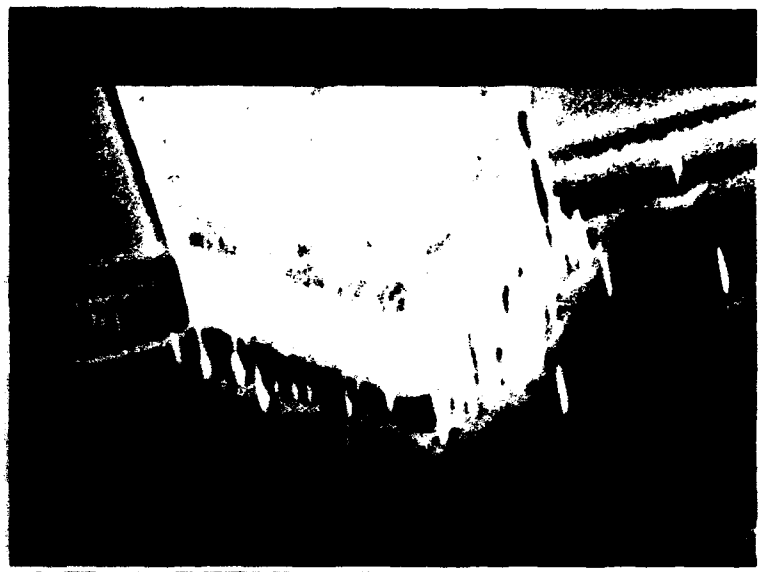

Figure 3. A total reflection mirror at the end of an etched ridge waveguide, as seen by a scanning electron microscope. The unintentional tree-like structures in the deeply etched region do not effect the performance of the mirror.

14. The wafers are now ready to be cleaved and tested. Even with etched laser mirrors, cleaving may be required in order to access the optical output.

Discussions of the test methods used as well as the design and testing of specific photonic circuits have been published separately.[1,10]

IV. Conclusion

Photonic circuits utilizing etched ridge waveguides in conjunction with deep etched mirrors can be fabricated in a self aligned process which avoids photo lithography on previously etched surfaces. This is accomplished by using an etch retarding mask to facilitate two etch depths during a single run in the CAIBE. Since the contact metallization and the un-etched region coincide, only two photo lithography masks are needed for this process.

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